Lamsim Enterprises inc.

White Paper

Heuristic Modeling of Transmission Lines due to Mixed Reference Plane Foil Roughness in Printed Circuit Board Stackups

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Abstract:

Designing the right printed circuit board stackup can make or break your product performance. If the product has circuitry that is impedance and transmission loss sensitive, then paying attention to conductor surface roughness is paramount. But sometimes the roughness of adjacent reference plane(s) is overlooked. If the adjacent high-speed signal layer is using smoother copper than one or both reference planes, a higher insertion loss than expected for that layer will occur and possibly cause your product to fail compliance. So how do we know this before finalizing the stackup? Since we do not have any empirical data to go by, we rely on heuristic modeling methods that rely solely on published parameters found in manufacturer's data sheets.

Table 1 Release Control Record[1]:

Issue 01	11/06/2021	Initial Release

[1] This document is an uncontrolled release. Latest issue can be obtained at LamsimEnterprises.com

Heuristic Modeling of Transmission Lines due to Mixed Reference Plane Foil Roughness in Printed Circuit Board Stackups

Designing the right printed circuit board (PCB) stackup can make or break your product performance. If your product has circuitry that is transmission loss sensitive, then paying attention to conductor surface roughness is paramount.

Conductor surface roughness traditionally has been applied to copper foil to promote adhesion to the dielectric material. Early PCBs were only constructed with single or double-sided copper core laminates. The only important metric for copper was its purity and the roughness to improve peel strength. There was no such thing as a PCB stackup and nobody worried about impedance or transmission line losses.

But over the years PCBs have evolved into multi-layer constructions with evermore attention being paid to impedance control and transmission line losses. Thus a PCB stackup definition became vital for consistent performance.

Like any construction project, you need a blueprint before you start building. Similarly for PCBs, you need a stackup drawing and detailed fabrication notes. Part of designing a stackup for today's high-performance designs requires consideration of the following:

- Choosing the right dielectric material for performance.
- Establishing finished core & prepreg thickness for accurate impedance modeling
- Choosing a glass style for better fiber weave effect mitigation
- Choosing the correct copper weight is important, to control voltage (IR) drop
- Specifying copper roughness to mitigate transmission line insertion loss

Part of the stackup design process includes signal integrity (SI) modeling for characteristic impedance and transmission loss. If your design is running at 56Gig pulse amplitude modulation level 4 (PAM-4), for example, you are probably looking at low loss dielectrics and low roughness copper for the signal traces.

But what is sometimes overlooked in the stackup, is the roughness of the reference planes. Often thin core laminate power and ground (GND) planes will specify reverse-treated foils (RTF), which are rougher on the side that bonds to the prepreg. Sometimes one of these planes, usually GND, acts as a reference plane to an adjacent signal layer as shown in Figure 1. If that adjacent high-speed signal layer is using smoother copper than one or both reference planes, a higher insertion loss than expected for that layer will occur and possibly ruin your day.

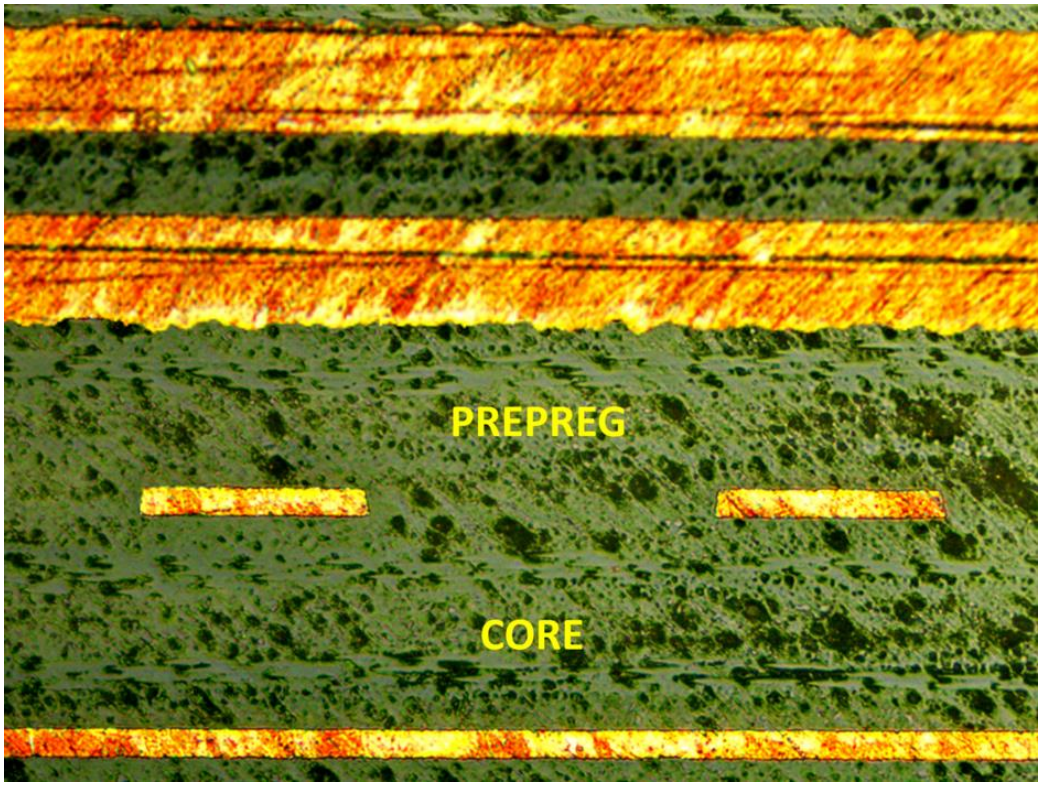


Figure 1 An example cross-section stripline geometry from a stackup showing thin core laminate (top) with RTF bonded to prepreg and adjacent to a high-speed differential pair with smooth foil.

A similar scenario could occur for high density interconnect (HDI) technology. This is a popular method to increase component density on modern PCBs. By the nature of their stackup construction, a rougher copper reference plane could sometimes also end up adjacent to a signal layer as well. Thus, if insertion loss is a concern, copper foil roughness of reference planes needs to be considered.

So how do you know this before you design your stackup and build your first prototype? Since we do not have any empirical data to go by, we rely on a heuristic, high-level design (HLD) modeling method starting with published parameters found solely in manufacturer's data sheets. Heuristic modeling is a practical technique that is not guaranteed to be perfect, but is still adequate in finding a satisfactory solution sooner, rather than later.

Background

PCB fab shops usually use a simple 2D field solver with Dk at 1-2 GHz to calculate characteristic impedance. One important parameter for accurate impedance modeling is dielectric constant (Dk). But since Dk is not constant over frequency, the HLD impedance modeling method determines Dkeff due to roughness, at or near the Nyquist frequency, which is one-half the Baud rate.

When doing SI impedance modeling, we need to get the dielectric material properties from the right sources. The best source is from laminate suppliers' data sheets. But there is an issue I like to think of as, "*a tale of two data sheets*".

Marketing data sheets, like the example shown on the left side of Figure 2, are easily found on laminate suppliers' websites. They are meant for quick comparison of dielectric parameters to narrow your search for the right laminate. But, they are not representative of what is needed to design an actual stackup. Depending on glass style, resin content and thickness, Dk and dissipation factor (Df) will be different and vary over frequency. So using numbers from these data sheets, will lead to inaccurate impedance results.

Instead, for HLD impedance and high-speed channel modeling, we need to use the same Dk/Df table data sheets, used by your PCB fab shop. An example is shown on the right side of Figure 2. They provide the actual core/prepreg thicknesses, resin content and Dk /Df over different frequencies for the different glass styles.

For Isola's Dk/Df table shown [5], Dk values are obtained using the Bereskin stripline test method for a specific group of constructions that represent the range of resin content of the composite. From that data set, the values for most of the constructions are calculated. Additional verification runs are performed to gather statistical data over time and validate the calculations are reasonable and accurate.

Property		Typical Values			
		Typical Value	Specification	Units Metric (English)	Test Method IPC-TM-650 (or as noted)
Glass Transition Temperature (Tg) by DSC		190	170-200	°C	2.4.25
Decomposition Temperature (Td) by TGA @ 5% weight loss		360	–	°C	ASTM D3850
T260		60	–	Minutes	ASTM D3850
T288		>30	–	Minutes	ASTM D3850
CTE, Z-axis	A. Pre-Tg B. Post-Tg	55 230	AABUS –	ppm/°C	2.4.24
CTE, X-, Y-axes	A. Pre-Tg B. Post-Tg	16 18	AABUS –	ppm/°C	2.4.24
Z-axis Expansion (50-260°C)		2.8	–	%	2.4.24
Thermal Conductivity		0.4	–	W/mK	ASTM D5930
Thermal Stress 10 sec @ 288°C (550.4°F)	A. Unetched B. Etched	Pass	Pass Visual	Rating	2.4.13.1
Dk, Permittivity (Laminate & prepreg as laminated) Tested at 50% resin	A. @ 100 MHz (HP4285A) B. @ 1 GHz (HP4291A) C. @ 2 GHz (Bereskin Stripline) D. @ 5 GHz (Bereskin Stripline) E. @ 10 GHz (Bereskin Stripline)	3.72 3.69 3.68 3.64 3.65	5.4 – – – –	–	2.5.5.3 2.5.5.9 2.5.5.5 2.5.5.5 2.5.5.5
Df, Loss Tangent (Laminate & prepreg as laminated) Tested at 50% resin	A. @ 100 MHz (HP4285A) B. @ 1 GHz (HP4291A) C. @ 2 GHz (Bereskin Stripline) D. @ 5 GHz (Bereskin Stripline) E. @ 10 GHz (Bereskin Stripline)	0.0072 0.0091 0.0092 0.0098 0.0095	0.035 – – – –	–	2.5.5.3 2.5.5.9 2.5.5.5 2.5.5.5 2.5.5.5
Volume Resistivity	A. 96/35/90 B. After moisture resistance C. At elevated temperature	– 4.4x10^7 9.4x10^7	1.0x10^6 – 1.0x10^3	MΩ-cm	2.5.17.1
Surface Resistivity	A. 96/35/90 B. After moisture resistance C. At elevated temperature	– 2.6x10^8 2.1x10^8	1.0x10^4 – 1.0x10^3	MΩ	2.5.17.1
Dielectric Breakdown		>50	–	kV	2.5.6
Arc Resistance		137	60	Seconds	2.5.1
Electric Strength (Laminate & prepreg as laminated)		70 (1741)	30 (750)	kV/mm (V/mil)	2.5.6.2
Comparative Tracking Index (CTI)		3 (175-249)	–	Class (Volts)	UL-746A ASTM D3638
Peel Strength	A. Low profile copper foil and very low profile – all copper weights >17 microns B. Standard profile copper 1. After thermal stress 2. At 125°C (257°F) 3. After process solutions	1.14 (6.5) – 0.96 (5.5) – 0.90 (5.1)	0.70 (4.0) – 0.80 (4.5) 0.70 (4.0) 0.55 (3.0)	N/mm (lb/inch)	2.4.8 2.4.8.2 2.4.8.3 – –
Flexural Strength	A. Lengthwise direction B. Crosswise direction	72,500 58,000	–	lb/inch^2	2.4.4
Tensile Strength	A. Lengthwise direction B. Crosswise direction	54,525 38,678	–	lb/inch^2	–
Young's Modulus	A. Grain direction B. Fill direction	3695 3315	–	ksi	ww
Poisson's Ratio	A. Grain direction B. Fill direction	0.137 0.133	–	–	xx
Moisture Absorption		0.061	–	%	2.6.2.1
Flammability (Laminate & prepreg as laminated)		V-0	–	Rating	UL 94
Max Operating Temperature		130	UL Cert	°C	–

The data, while believed to be accurate and based on analytical methods considered to be reliable, is for information purposes only. Any sales of these products will be governed by the terms and conditions of the agreement under which they are sold.

Dielectric Constant(Dk) / Dissipation factor (Df) Table

Core Data

Construction	Resin Content %	Standard/ Alternate	Thickness (inch)	Thickness (mm)	Dielectric Constant (DK)/ Dissipation Factor (DF) 100 MHz	500 MHz	1 GHz	2 GHz	5 GHz	10 Ghz
1x106	72.0%	Standard	0.0020	0.051	3.37 0.0075	3.36 0.0089	3.34 0.0096	3.32 0.0101	3.30 0.0107	3.30 0.0107
1x1080	57.0%	Standard	0.0025	0.064	3.67 0.0071	3.64 0.0079	3.62 0.0089	3.61 0.0092	3.60 0.0097	3.59 0.0095
1x1067	69.0%	Alternate	0.0025	0.064	3.42 0.0075	3.40 0.0084	3.38 0.0095	3.36 0.0100	3.34 0.0105	3.33 0.0104
1x1080	63.0%	Standard	0.0030	0.076	3.54 0.0074	3.52 0.0082	3.50 0.0092	3.48 0.0096	3.47 0.0102	3.47 0.0101
1x1086	59.0%	Alternate	0.0030	0.076	3.65 0.0072	3.63 0.0079	3.60 0.0091	3.59 0.0092	3.57 0.0098	3.57 0.0095
2x106	67.0%	Standard	0.0035	0.089	3.46 0.0074	3.45 0.0083	3.42 0.0094	3.40 0.0098	3.38 0.0104	3.37 0.0102
1x3313	51.0%	Standard	0.0035	0.089	3.82 0.0068	3.79 0.0076	3.77 0.0084	3.77 0.0087	3.74 0.0092	3.74 0.0090
1x106/1x1080	59.0%	Standard	0.0040	0.102	3.63 0.0072	3.61 0.0080	3.58 0.0090	3.57 0.0093	3.55 0.0098	3.54 0.0096
1x3313	55.0%	Standard	0.0040	0.102	3.72 0.0071	3.70 0.0077	3.68 0.0087	3.66 0.0090	3.65 0.0095	3.65 0.0094
1x106/1x1080	61.0%	Alternate	0.0043	0.109	3.57 0.0073	3.56 0.0081	3.54 0.0092	3.52 0.0095	3.51 0.0099	3.50 0.0098
1x2116	50.0%	Standard	0.0045	0.114	3.82 0.0068	3.81 0.0075	3.80 0.0083	3.79 0.0086	3.78 0.0091	3.76 0.0089
1x106/1x1080	62.0%	Standard	0.0045	0.114	3.55 0.0073	3.54 0.0082	3.52 0.0092	3.50 0.0095	3.48 0.0100	3.48 0.0098
2x1067	69.0%	Alternate	0.0050	0.127	3.42 0.0075	3.40 0.0084	3.38 0.0095	3.36 0.0100	3.34 0.0105	3.33 0.0104
2x1080	57.0%	Standard	0.0050	0.127	3.67 0.0071	3.64 0.0079	3.62 0.0089	3.61 0.0092	3.60 0.0097	3.59 0.0095
1x2116	54.0%	Standard	0.0050	0.127	3.72 0.0070	3.71 0.0077	3.70 0.0086	3.69 0.0089	3.67 0.0095	3.67 0.0093
2x1080	58.0%	Standard	0.0055	0.140	3.65 0.0072	3.63 0.0079	3.60 0.0091	3.59 0.0092	3.57 0.0098	3.57 0.0095
2x1086	58.0%	Alternate	0.0060	0.152	3.65 0.0072	3.63 0.0079	3.60 0.0091	3.59 0.0092	3.57 0.0098	3.57 0.0095
1x1652	50.0%	Standard	0.0060	0.152	3.82 0.0068	3.81 0.0075	3.80 0.0083	3.79 0.0086	3.78 0.0091	3.76 0.0089

Figure 2 Left - an example of manufacturer's data sheet easily found on laminate supplier's web site. Right - example of Dk/Df table used for stackup and impedance modeling. Source: Isola Group [5]

Many engineers assume Dk published is the intrinsic property of the material. But in actual fact, it is the effective Dk (Dkeff) measured by a specific test method. When simulations are compared against measurements, there is often a discrepancy in Dkeff, due to increased phase delay caused by surface roughness.

Dkeff is highly dependent on the test apparatus and conditions of how it is measured. One method commonly used by many laminate suppliers is the clamped stripline resonator test method, as described by IPC-TM-650, 2.5.5.5, Rev C, Test Methods Manual [17].

The measurements are done under stripline conditions using a carefully designed resonant element pattern card made with the same dielectric material to be tested. As shown in Figure 3, the card is sandwiched between two sheets of unclad dielectric material under test. Then the whole structure is clamped between two large plates; each lined with copper foil and are grounded. They act as reference planes for the stripline.

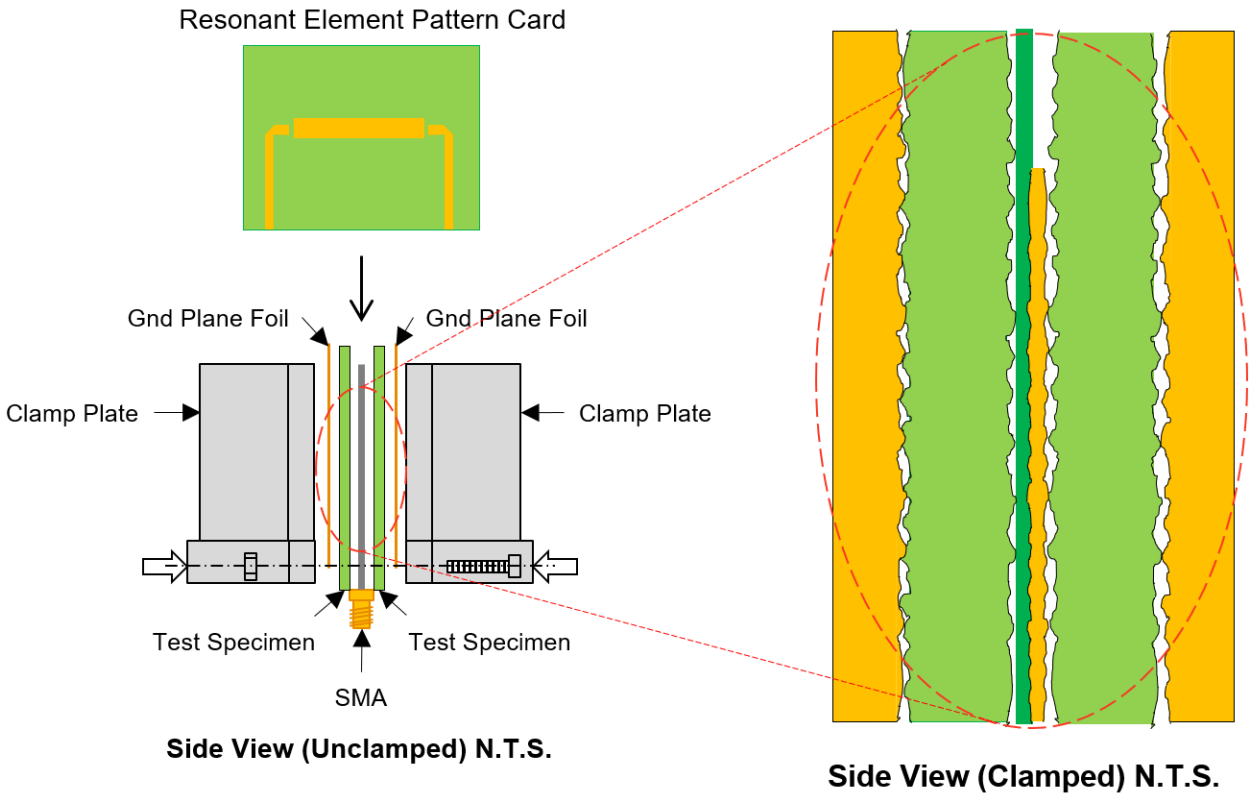


Figure 3 Illustration of clamped stripline resonator test method, as described by IPC-TM-650, 2.5.5.5, Rev C, Test Methods Manual.

This test method assures consistency of product when used in fabricated boards. It does not guarantee the values directly correspond to design applications. Here's why:

Since the resonant element pattern card and material under test are not physically bonded together, air is entrapped between the various layers. The small air gaps result in a lower effective Dk than

what is measured with rougher foil bonded to the same core laminate. This is the primary reason for phase delay discrepancy between simulation and measurements.

When copper foil with the same roughness is bonded to each side of the core or prepeg, Dk is adjusted using this simple Dkeff correction factor [4]:

Equation 1

$$Dkeff \approx \frac{H_{smooth}}{\left(H_{smooth} - 2Rz\right)} \times Dk$$

where:

H_{smooth} is dielectric core or pressed prepreg thickness; Rz is conductor roughness of the foil; Dk is dielectric constant from laminate supplier's Dk/Df tables.

But when copper roughness is different on each side of the core or prepreg, like the example shown in Figure 1, Dkeff correction factor is determined by:

Equation 2

$$Dkeff \approx \frac{H_{smooth}}{\left(H_{smooth} - \left(Rz_1 + Rz_2\right)\right)} \times Dk$$

where:

Rz_1 and Rz_2 are the conductor roughness of the foil for the respective side of the dielectric. In the example shown in Figure 1, Rz_1 is the roughness for the top RTF reference plane and Rz_2 is the roughness of the top surface of adjacent signal traces bonded to prepreg.

HLD Transmission Line Loss Modeling

The HLD transmission line loss modeling is a heuristic approach using material parameters solely from manufacturers' data sheets. For dielectric parameters, we choose Dk/Df at or near the Nyquist frequency of the baud rate, then apply Dkeff correction factor due to roughness. For conductor loss we use Rz roughness numbers from copper suppliers' data sheets and oxide/oxide alternative treatments, used by your favorite fab shop.

A more sophisticated 2D/2.5D or 3D field solver is required with adequate conductor roughness models included. Popular roughness models in many EDA tools and field solvers include, Hammerstad-Jensen, Huray, or the more recent, Cannonball-Huray roughness model I developed [1]-[2].

Cannonball-Huray Model

The Cannonball model allows you to extract the right parameters needed for the popular Huray model simply from manufacturers' data sheets. As illustrated in Figure 4, there are three rows of

equal sized spheres stacked on a square tile base. Nine spheres are on the first row, four spheres in the middle row, and one sphere on top. This stacking arrangement is known as close-packing of equal spheres, but more commonly known as the *"Cannonball"* stack due to the method used by sailors to stack actual cannonballs aboard ships.

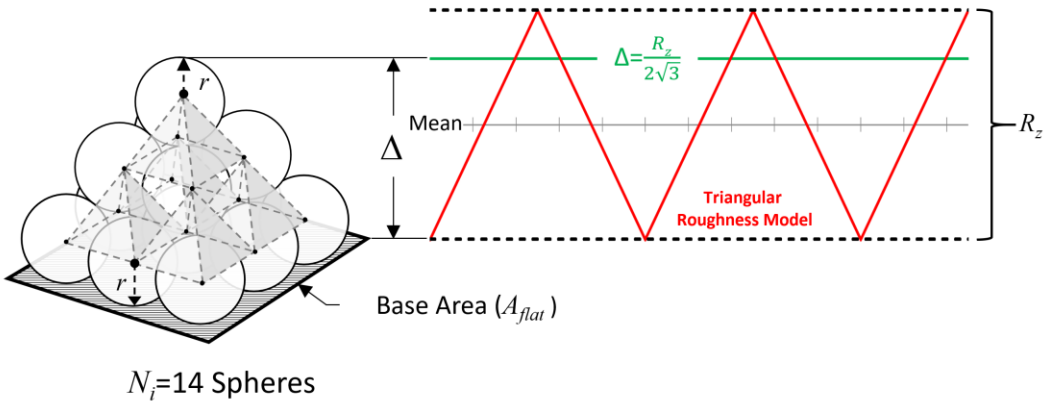


Figure 4 Cannonball-Huray physical model. The height of the stack is the RMS height of the peak to valley profile equal to Rz from data sheets

Given the height of the Cannonball stack (Δ), is equal to the RMS value of the peak to valley triangular roughness profile; then from method described in [1], determining the sphere radius (*r*) from Rz roughness parameters found in data sheets, can be further simplified and approximated as [3]:

Equation 3

$$r \approx 0.06\text{Rz}$$

and base area (A_{flat}) as:

Equation 4

$$A_{flat} \approx 36(r)^2$$

Because the model assumes the ratio of A_{matte}/A_{flat} = 1, and there are only 14 spheres, the Cannonball-Huray model can be further simplified to:

Equation 5

$$K_{CH}(f) \approx 1 + 2.33\pi\left(1 + \frac{\delta(f)}{r} + \frac{\delta^2(f)}{2r^2}\right)^{-1}$$

where:

$K_{CH}(f)$ = Cannonball-Huray roughness correction factor, as a function of frequency; $\delta(f)$ = skin-depth, as a function of frequency in meters; r = the radius of spheres in meters (Equation 3).

As can be seen, the radius is the only parameter needed, which can be easily determined by Rz. The beauty of the Cannonball-Huray model is that it offers the simplicity of the Hammerstad model, but has the accuracy of the original Huray model. So if you are used to using the Hammerstad model in your work flow, you should find this model just as easy to use.

Wildriver Isola I-Tera® MT40 Custom Modeling Platform Case Study

To study the effect of reference plane roughness on transmission insertion loss, Wildriver Technology's [6] custom modeling platform (CMP), shown in Figure 5, was used as a case study. This CMP was custom developed for Isola [5] to characterize their new I-Tera® MT40 very low-loss laminate material.

It combines 27 structures based on a consistent development of primitive structures; useful for performing a host of calibrations including automatic fixture removal, unknown THRU, WinCal XE™ calibration, and VNA gating and time transform analysis.

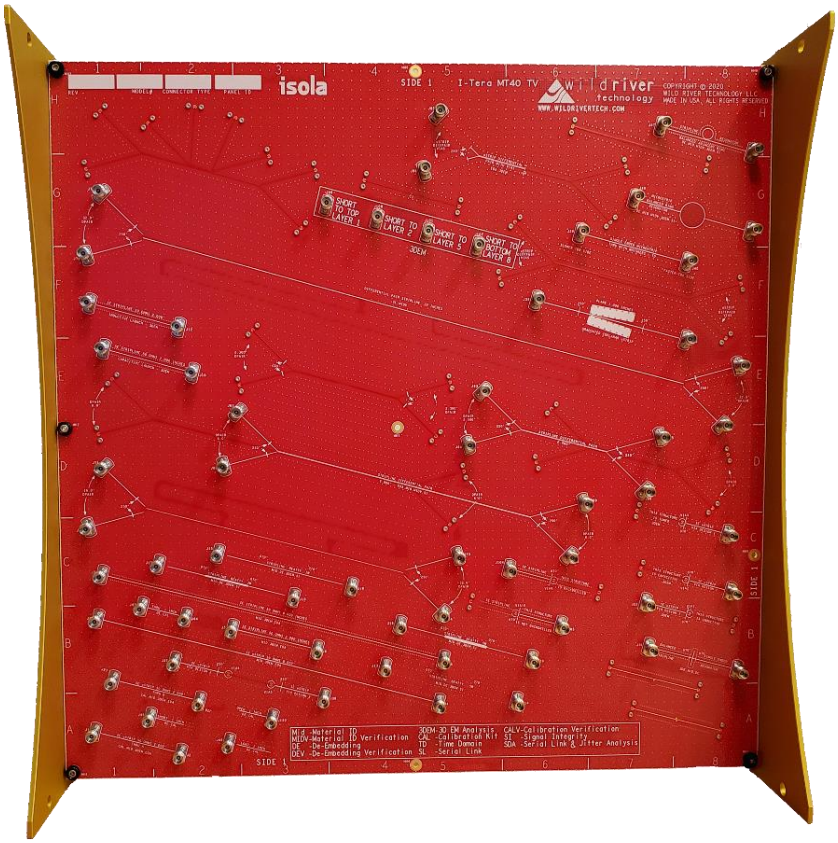


Figure 5 Wildriver Isola I-Tera® MT40 Custom Modeling Platform. Source: Wildriver Technology [6]

Stackup Validation

The PCB stackup is shown in Figure 6. Often PCB fab shop field application engineers (FAE) modify existing stackups and unintentionally make errors in transferring new parameters from data sheets into their software tools.

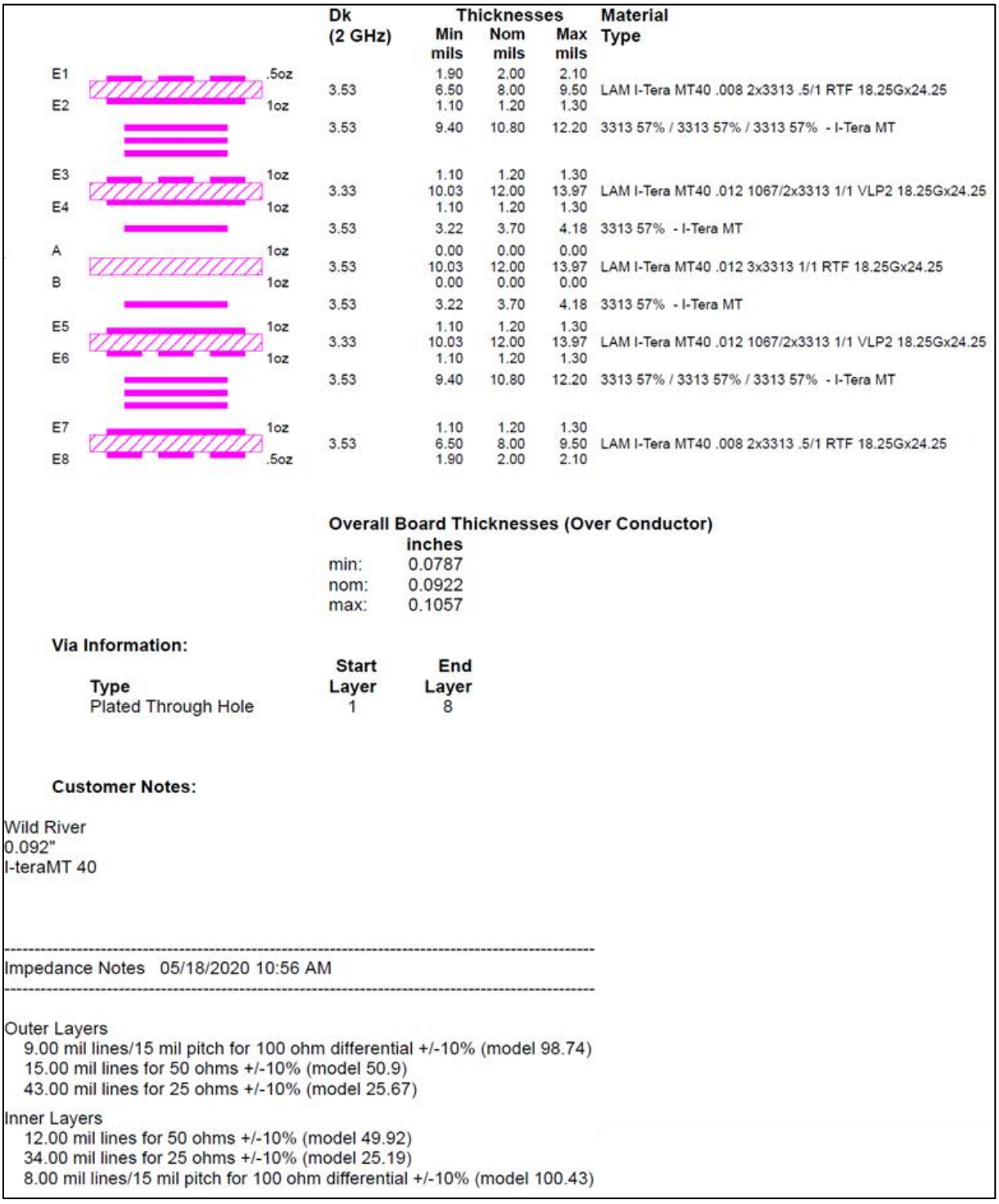
So the first step I like to do in any model correlation exercise is to sanitize the stackup, to ensure it meets the product design intent for signal integrity (SI) performance. In fact that is how the issue of different plane roughness was uncovered.

Since I always ensure the same roughness is specified for reference planes as the adjacent signal layers, I naively assumed it would be the case for any high-speed stackup. The fab shop FAE may not necessarily know the design intent of the stackup, so it is always good practice for SI engineers to review the stackup before final design files are released.

As we can see, layers E1,E2 and E7, E8 specify 1oz RTF, while layers E3, E4 and E5, E6 specify 1oz VLP2 foil. Because the Isola I-Tera® MT40 CMP is intended to aid in modeling test structures, this is not a fatal flaw. But it is a perfect platform to demonstrate the HLD modeling methodology and assess the effect of rougher reference planes.

The next step is validating all other relevant impedance modeling parameters against the Dk/Df tables for the material specified. In this cases study, the dielectric Dk/Df tables are found in the Appendix along with the foil supplier's data sheets for the different foils offered for I-Tera® MT40 laminates.

The stackup offers two signal routing layers, so we are interested in the respective core and prepreg parameters. Upon review, it was discovered that the core laminates between E3,E4 and E5, E6 specified 1067/2x3313 glass styles, but this core is not listed in the Dk/Df table for 12 mil thickness. Instead, only 3x3313 core is offered. Because of that, the Dk shown is also wrong and will affect the impedance of the traces. The right Dk for 3x3313 is 3.53 instead if 3.33.



		Dk (2 GHz)	Thicknesses Min mils	Nom mils	Max mils	Material Type
E1	.5oz		1.90	2.00	2.10	
		3.53	6.50	8.00	9.50	LAM I-Tera MT40 .008 2x3313 .5/1 RTF 18.25Gx24.25
E2	1oz		1.10	1.20	1.30	
		3.53	9.40	10.80	12.20	3313 57% / 3313 57% / 3313 57% - I-Tera MT
E3	1oz		1.10	1.20	1.30	
		3.33	10.03	12.00	13.97	LAM I-Tera MT40 .012 1067/2x3313 1/1 VLP2 18.25Gx24.25
E4	1oz		1.10	1.20	1.30	
		3.53	3.22	3.70	4.18	3313 57% - I-Tera MT
A	1oz		0.00	0.00	0.00	
		3.53	10.03	12.00	13.97	LAM I-Tera MT40 .012 3x3313 1/1 RTF 18.25Gx24.25
B	1oz		0.00	0.00	0.00	
		3.53	3.22	3.70	4.18	3313 57% - I-Tera MT
E5	1oz		1.10	1.20	1.30	
		3.33	10.03	12.00	13.97	LAM I-Tera MT40 .012 1067/2x3313 1/1 VLP2 18.25Gx24.25
E6	1oz		1.10	1.20	1.30	
		3.53	9.40	10.80	12.20	3313 57% / 3313 57% / 3313 57% - I-Tera MT
E7	1oz		1.10	1.20	1.30	
		3.53	6.50	8.00	9.50	LAM I-Tera MT40 .008 2x3313 .5/1 RTF 18.25Gx24.25
E8	.5oz		1.90	2.00	2.10	

Overall Board Thicknesses (Over Conductor)

	inches
min:	0.0787
nom:	0.0922
max:	0.1057

Via Information:

Type	Start Layer	End Layer
Plated Through Hole	1	8

Customer Notes:

Wild River
0.092"
I-teraMT 40

Impedance Notes 05/18/2020 10:56 AM

Outer Layers
9.00 mil lines/15 mil pitch for 100 ohm differential +/-10% (model 98.74)
15.00 mil lines for 50 ohms +/-10% (model 50.9)
43.00 mil lines for 25 ohms +/-10% (model 25.67)

Inner Layers
12.00 mil lines for 50 ohms +/-10% (model 49.92)
34.00 mil lines for 25 ohms +/-10% (model 25.19)
8.00 mil lines/15 mil pitch for 100 ohm differential +/-10% (model 100.43)

Figure 6 Isola I-Tera® MT40 Custom Modeling Platform stackup from PCB fab shop . Source: Wildriver Technology [6]

After the stackup is sanitized, the as-specified impedance for trace geometries needs to be verified using a field solver. In this case, we will be modeling and correlating the 15 mil, 50 ohm single-ended (SE) trace; but normally all impedance geometries would be sanitized.

Polar Instruments SI9000 field solver, was used to compare the as-specified stackup geometry against one with corrected Dk. Figure 7 left shows the impedance of 49.5 ohms using stackup Dk parameters. But when Dk for a 3x3313 core was used, the impedance difference is less than an ohm.

Figure 7 Comparison of characteristic impedance for 50-ohm trace using Dk for 1067/2x3313 core from stackup drawing vs Dk for 3x3313 from Dk/Df tables

Foil Roughness

As mentioned earlier, the roughness of the foil affects the effective Dk, so we need to use the right number for our model validation. The standard VLP2 foil, used on I-Tera® MT40 core laminates is BF-TZA foil. Optional RTF foil, used for layers E1, E2 and E7, E8, is TWLS-B. Both are from Circuit Foil [7], and their full data sheets are found in the Appendix.

Relevant roughness parameters are shown in Figure 8. For the core side of the foil we are interested in the Rz parameters for the treated side listed in the table. But there are two Rz parameters, JIS B 601 and ISO 4287 for the treated side specified. So which one do we use for modeling?

From IPC-TM-650 Section 1.2 [16] states, "*The foil profile of foils shall be evaluated using the parameter Rz (DIN) or RTM, which is defined as the average maximum peak to valley height of five consecutive sampling lengths within the measurement length. This value is approximately equivalent to the values of profile determined from microsectioning techniques.*"

and;

Section 1.3 states, "*RZ (ISO) is a different parameter from Rz (DIN) and is not applicable to this method.*"

BF-TZA

MEASURED PARAMETERS			UNITS	PRODUCT GAUGE					IPC	
Nominal Thickness			**µm oz.**	**9 1/4**	**12 3/8**	**18 1/2**	**35 1**	**70 2**	**Specification IPC-4562A**	**Test Method IPC-TM-650**
Area Weight			g/m²	79	112	152	285	574	3.4.4	2.2.12
Untreated Side Contact Roughness	Ra	ISO 4287	µm	≤ 0.35					3.5.6	2.2.17
Untreated Side Contactless Roughness	Sa	ISO 25178	µm	~ 0.22					-	2.2.22 Draft[2]
Treated Side Contact Roughness	Rz	JIS B 601	µm	≤ 2.5				≤ 2.0	-	2.2.17
	Rz	ISO 4287	µm	≤ 3.1				≤ 2.5	3.4.5	
Treated Side Contactless Roughness	Sa	ISO 25178	µm	~ 0.42	~ 0.38	~ 0.35	~ 0.31	~ 0.26	-	2.2.22 Draft[2]
	Sz		µm	~ 4.7	~ 4.4	~ 4.1	~ 3.7	~ 3.3		
	Sdr		%	~ 12	~ 11.5	~ 11	~ 10.5	~ 10		
Tensile Strength Transverse (RT)			MPa (k.Lb/in²)	≥ 276 (≥ 40)					3.5.1	2.4.18
Elongation Transverse (RT)			%	4 - 14	5 - 15	7 - 25	10 - 35	15 - 40	3.5.3	
Peel Strength Very Low Loss (PPE Based Resin)[1] (RT)			N/mm (Lb/in)	≥ 0.6[3] (≥ 3.4)	≥ 0.45 (≥ 2.6)	≥ 0.5 (≥ 2.9)	≥ 0.6 (≥ 3.4)	≥ 0.7 (≥ 4.0)	3.5.4	2.4.8

[1] Laminate construction with thickness ≥ 0.5 mm
[2] Final draft of TM 2.2.22 as of Sept. 29th, 2015
[3] After build-up to 35 µm

TWLS-B

MEASURED PARAMETERS		UNITS	PRODUCT GAUGE			IPC	
Nominal Thickness		**µm oz.**	**18 1/2**	**35 1**	**70 2**	**Specification IPC-4562A**	**Test Method IPC-TM-650**
Area weight		g/m²	157	287	577	3.4.4	2.2.12
Untreated Matte Side Roughness (Rz)	JIS	µm	≤ 5.0	≤ 7.5	≤ 9.2	-	2.2.17
	ISO	µm	≤ 6.0	≤ 9.0	≤ 11.0	3.4.5	
Treated Shiny Side Roughness (Rz)	JIS	µm	≤ 4.2			-	
	ISO	µm	≤ 5.1			3.4.5	
Tensile Strength Transverse (RT)		MPa (k.Lb/in²)	≥ 276 (≥ 40)			3.5.1	2.4.18
Tensile Strength Transverse (180 °C)		MPa (k.Lb/in²)	≥ 138 (≥ 20)				
Elongation Transverse (RT)		%	≥ 6	≥ 9	≥ 12	3.5.3	
Elongation Transverse (180 °C)		%	≥ 3				
Peel Strength Filled Hydrocarbon Resin[1] (RT)		N/mm (Lb/in)	≥ 0.5 (≥ 2.9)	≥ 0.6 (≥ 3.4)		3.5.4	2.4.8

[1] Laminate construction with thickness ≥ 0.5 mm

Figure 8 Roughness parameters from Circuit Foil [7] data sheets. Top is VLP2 standard foil used on I-Tera® MT40, while bottom is RTF option used for relevant layers in the stackup

RzJIS represents the 10-point mean value, which is the sum of the average of the 5 highest peaks and the 5 lowest valleys over the sample length. RzDIN is similar; except it is defined as the average maximum peak to valley height of five consecutive sampling lengths within the measurement length.

Thus we will use RzJIS for modeling analysis.

Oxide/Oxide Alternative Roughness Treatment

Oxide treatment involves growing copper oxide crystals on the surface of the copper to add roughness. Since the oxide is virtually non-conductive, the oxide crystals do not significantly affect the transmission loss. Oxide alternative (OA) treatments, on the other hand, involves an etching process which changes the underlying copper surface profile and thus can significantly affect the transmission loss.

In 2016 the High-density Packaging User Group (HDPUG) [10] undertook a project to evaluate the high frequency loss impacts of a variety of OA treatments on a Megtron-6 (Meg-6) HVLP test platform. From that study, three popular manufacturer OA treatments, referred to as A,B,C, were analyzed.

Table 2 summarizes the respective Rq/Rz roughness values compared to base copper (CU) roughness.

Table 2 Comparison of Rq/Rz copper surface roughness measurements after OA treatment from HDPUG study [10]

OA Sample	Rq µm	*Rz µm
Base CU	0.305	1.06
A	0.547	1.89
B	0.548	1.89
C	0.440	1.52
*Rz $\approx$ Rq$(2\sqrt{3})$ Ref: [3]		

Normally the treated matte side of the foil gets bonded to the core laminate by the laminate supplier. An oxide or OA treatment is usually applied by the PCB fabricator to the copper surfaces bonding to the prepreg side prior to final PCB lamination. For most cases, this treatment is applied to the untreated drum (smooth) side of the foil.

The opposite is true for RTF. In this case, the treated drum side is bonded to the core by laminate supplier, while the rougher matte side of the foil gets treated with oxide or OA by the PCB fabricator.

When it is applied to the matte side of RTF, it tends to smoothen the macro-roughness slightly [9]. At the same time, it creates a surface full of micro-voids, which follows the underlying rough profile and allows the resin to fill in the cavities. Thus providing a good mechanical bond to the prepreg. Typically 50 µin (1.27µm) of copper is removed when the treatment is completed, depending on the board shop's process control [18]. Because actual OA alternative roughness

numbers are difficult to obtain from OA supplier's, the HLD modeling methodology uses worst case A (Rz ~ 1.9 μm) for untreated drum sides of the foil from Table 2.

If oxide treatment is applied instead, we use the base copper roughness (Rz = 1.1μm) from Table 2.

For RTF, we use the matte side Rz roughness from foil data sheet minus 50 μin (1.27 μm) for untreated drum side of the foil.

Determine Effective Dk Due to Roughness

The first step in HLD impedance modeling is to gather all the dielectric and foil data sheet parameters to determine the effective Dk.

Figure 9 summarizes thickness of core, prepreg and signal trace from the stackup geometry in Figure 6. Note that photos are for illustrative purposes only and are not actual cross-sections from CMP PCB. Dk for core and prepreg were obtained from Dk/Df tables found in the Appendix.

The top reference plane is TWLS-B RTF foil with matte side $Rz1 \leq 7.5um$ JIS, obtained from the data sheet in Figure 9. The roughness surface profile is shown in the upper left. After OA smoothing, $Rz1 \leq 6.23um$.

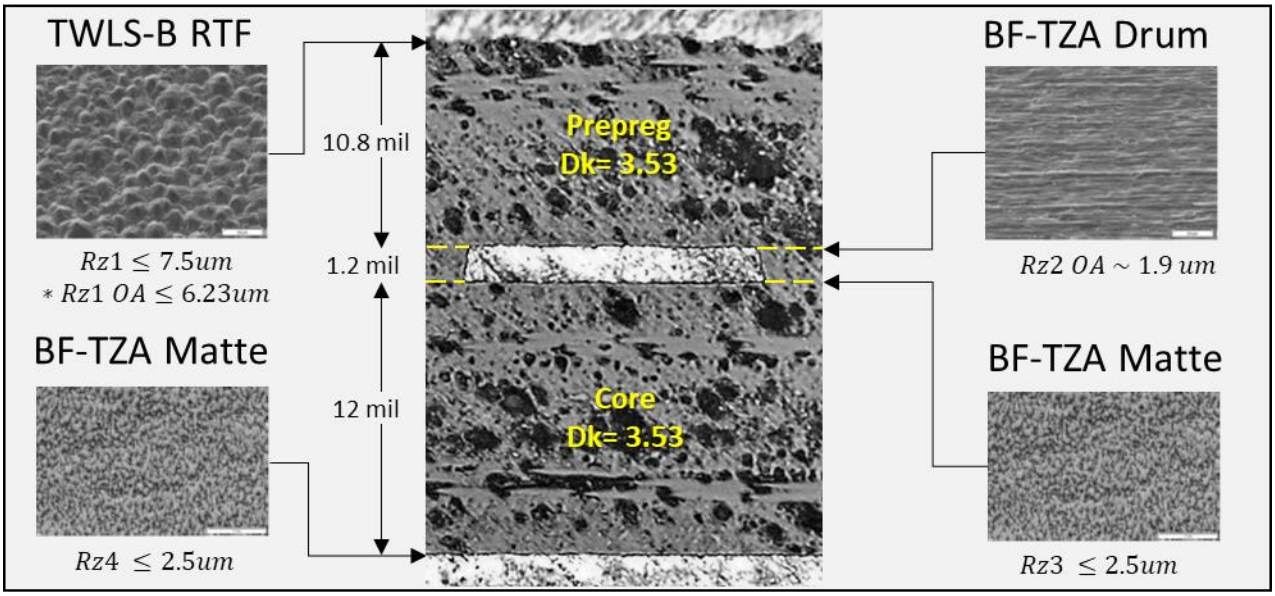
BF-TZA foil is used for both sides of the core laminate. The top surface of the stripline trace, shown in the upper right picture, is the drum side of the foil, before OA treatment. Since we don't know the fab shop's OA treatment, we use OA sample A (Rz2 ~ 1.9 μm), from Table 2.

The bottom surface profile of the stripline trace and the top surface of the bottom reference plane are the treated matte sides of the foil, shown in the bottom right and bottom left pictures respectively. They both share the same roughness (Rz3, Rz4 ≤ 2.5μm JIS) from the BF-TZA data sheet shown in Figure 9.

The next step is to convert the imperial thickness units to metric, then use Equation 2 to determine Dkeff due to roughness for the prepreg and core.

$$Dkeff_{prepreg} \approx \frac{H_{prepreg}}{\left(H_{prepreg} - \left(Rz_1 + Rz_2\right)\right)} \times Dk \approx \frac{274.32um}{\left(274.32um - \left(6.23um + 1.9um\right)\right)} \times 3.53 \approx 3.64$$

$$Dkeff_{core} \approx \frac{H_{core}}{\left(H_{core} - \left(Rz_3 + Rz_4\right)\right)} \times Dk \approx \frac{304.8um}{\left(304.8um - 2\left(2.5um\right)\right)} \times 3.53 \approx 3.59$$



* Rz1 after 50uin (1.27um) OA smoothing

Figure 9 Data sheet parameters for RTF/VLP2 foil roughness and dielectric properties for I-Tera® MT40 stackup geometry. Note: Photos are for illustrative purposes only and are not actual cross-sections from CMP PCB. Surface roughness pictures source: Circuit Foil [7]

Determine Cannonball-Huray Roughness Parameters

Several popular electronic design automation (EDA) tools ask for input parameters for the Huray model that are not easily apparent unless you go searching in their help manual.

Popular tools like Mentor Hyperlynx [14] and Polar Instruments Si9000e [8] include the Cannonball-Huray model directly as an option, so all that needs to be entered is Rz of the foil directly.

Ansys (HFSS) [12] and Cadence [13] tools require surface ratio (*sr*) and nodule radius (*r*) as input parameters. In this context, surface ratio is defined as surface area of spheres divided by the base area. Nodule radius (*r*) is calculated from Equation 3.

Because the Cannonball model always has *N*=14 spheres and base area (A_{flat}) is always $36r^2$, r^2 cancels out and *sr* can be simplified to a constant per the following equation:

Equation 6

$$sr = \left(\frac{N \times 4\pi r^2}{A_{flat}}\right) = \left(\frac{14 \times 4\pi r^2}{36r^2}\right) = \left(\frac{14 \times 4\pi}{36}\right) = 1.56\pi \approx 4.9$$

Simbeor electromagnetic signal integrity software tool, from Simberian Inc.[15], requires two parameters; roughness factor (*RF1*) and sphere radius (*SR1)*. Similarly, (A_{flat}) is always $36r^2$, so r^2 cancels out and *RF1* can be simplified to a constant per the following equation:

Equation 7

$$RF1 = 1 + \frac{3}{2}\left(\frac{N \times 4\pi r^2}{A_{flat}}\right) = 1 + \frac{3}{2}\left(\frac{14 \times 4\pi (r_{avg})^2}{36(r_{avg})^2}\right) \approx 8.33$$

If your tool allows for inputting roughness parameters for each surface of the geometry then the next step is to determine the sphere radius, (r) and (A_{flat}), if your tool asks for that parameter.

So, referring back to Figure 9, the following procedure calculates both for each surface:

$$r_1 = 0.06\left(Rz_1\right) = 0.06\left(6.23um\right) = 0.374um$$
$$A_{flatt1} = 36\left(r_1\right)^2 = 5.03um^2$$

$$r_2 = 0.06\left(Rz_2\right) = 0.06\left(1.9um\right) = 0.114um$$
$$A_{flatt2} = 36\left(r_2\right)^2 = 0.467um^2$$

$$r_3 = 0.06\left(Rz_3\right) = 0.06\left(2.5um\right) = 0.150um$$
$$A_{flatt3} = 36\left(r_3\right)^2 = 0.81um^2$$

$$r_4 = 0.06\left(Rz_4\right) = 0.06\left(2.5um\right) = 0.150um$$
$$A_{flatt4} = 36\left(r_4\right)^2 = 0.81um^2$$

Any of these tools can be used for HLD modeling, but my favorite is Polar SI9000 because of its simplicity and sufficient accuracy for prefabrication modeling and analysis. Many fab shops use this tool for impedance modeling, so it is easy to stay in sync with them during the high-level design stage of your project. Plus, it has the added benefit of modeling transmission loss and outputting S-parameters in touchstone format for further channel modeling in other tools.

Because Polar Si9000 assumes all the reference planes have the same roughness, it only allows Rz roughness parameters to be inputted for the matte and drum side of the signal trace. The best we can do, is take the average roughness of Rz3,Rz4 and Rz1,Rz2 respectively:

$$Rz_{drum} = 0.5\left(Rz_1 + Rz_2\right) = 0.5\left(6.23um + 1.9um\right) = 4.07um$$
$$Rz_{matte} = 0.5\left(Rz_3 + Rz_4\right) = 0.5\left(2.5um + 2.5um\right) = 2.50um$$

HLD Simulation Correlation

The first thing to do is replace the data sheet values for Dk, with Dkeff due to roughness. When we do this, the new impedance prediction, shown in Figure 10, is 48.24 ohms.

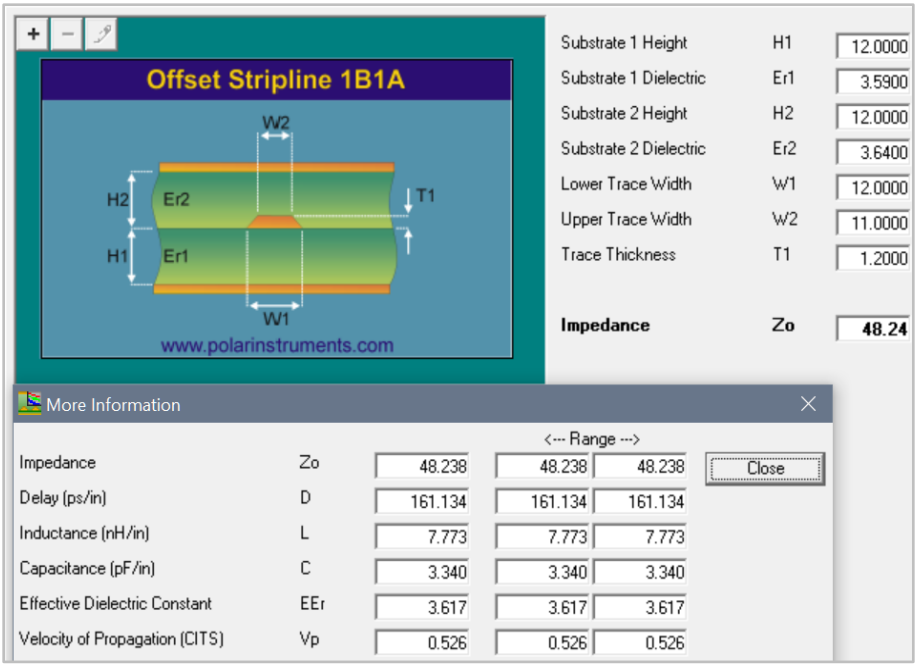


Figure 10 Polar Si9000 impedance prediction with Dkeff due to roughness

Next we input Dkeff/Df for H1, H2 into the causal dielectric model at 10GHz, as shown in Figure 11 (left). Then we input Rz_{matte}, Rz_{drum} into the Cannonball-Huray model (right).

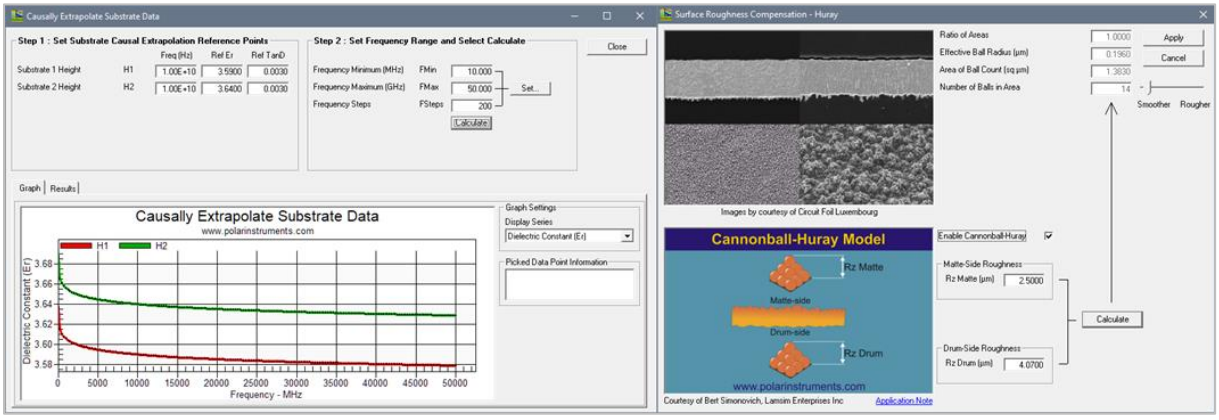


Figure 11 Causal Dkeff/Df dielectric and Cannonball-Huray roughness model input panels in Polar Si9000

After simulation for 6-inch transmission line, the S-parameters were exported in touchstone format. Then it was imported into Keysight Pathwave ADS [11], for further processing and analysis.

Figure 10 compares simulated insertion loss vs GMS de-embedded S-parameter measurements, provided by Wildriver Technology [6]. As you can see there is excellent correlation without fitting to measured data!

Figure 12 HLD Insertion Loss simulation correlation for as designed stackup from data sheet and stackup parameters

Phase delay, also known as time delay (TD) in seconds, can be derived from the transmission phase angle, and is used as a metric for simulation correlation accuracy. TD, as a function of frequency, is calculated from the unwrapped measured transmission phase angle, and is given by:

Equation 8

$$TD(f) = -1\left[\frac{unwrap(phase(S21))}{360 \times freq}\right]$$

Dkeff, as a function of frequency, is then determined by:

Equation 9

$$D_{keff}(f) = \left(TD(f)\frac{c}{Length}\right)^2$$

where:

c = speed of light in *m/s*; *Length* = length of conductor in meters.

Figure 13 plots simulated Dkeff vs measurements. At 10 GHz, simulated Dkeff is 0.105 (-2.8%) lower than measured value. Without actual cross-section microscopic measurements, it is difficult to conclude if the published Dk is wrong, or if there is process variation with roughness parameters used in the model.

But it is also interesting to note that measured Dkeff is not a constant value over frequency, as shown in the I-Tera® MT-40 Dk/Df tables. Instead it varies over frequency, so the Dk/Df data sheet numbers are suspect.

Regardless, for the HLD modeling process, the simulation results are within acceptable tolerance.

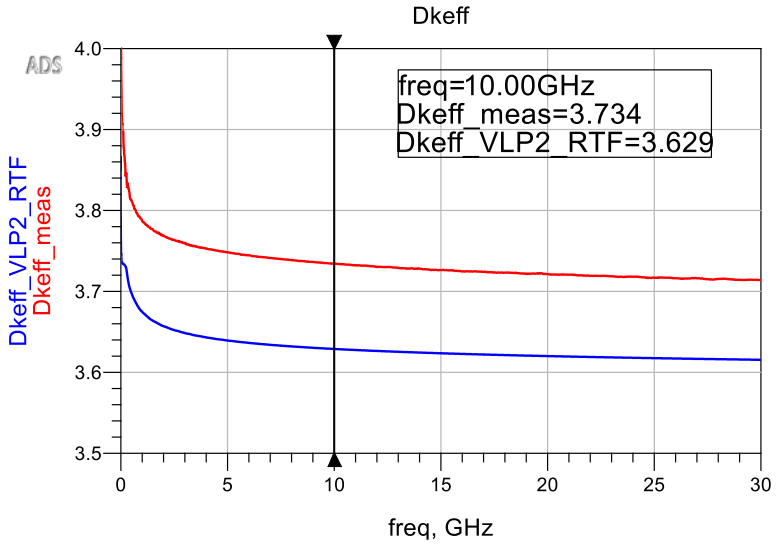


Figure 13 HLD Dkeff simulation correlation for as designed stackup

Exploring the Effects of Alternate Foil Roughness

Now that we have good correlation to measurements, we can repeat the HLD modeling process to explore different foil roughness options. Figure 14 summarizes the thickness of core, prepreg and signal trace for VLP2/VLP2 foil (top) and VLP1/VLP1 foil (bottom). Note that photos are for illustrative purposes only and are not actual cross-sections from CMP PCB.

Respective Dkeff, and Cannonball-Huray roughness parameters were recalculated with same steps as VLP2/RTF case above.

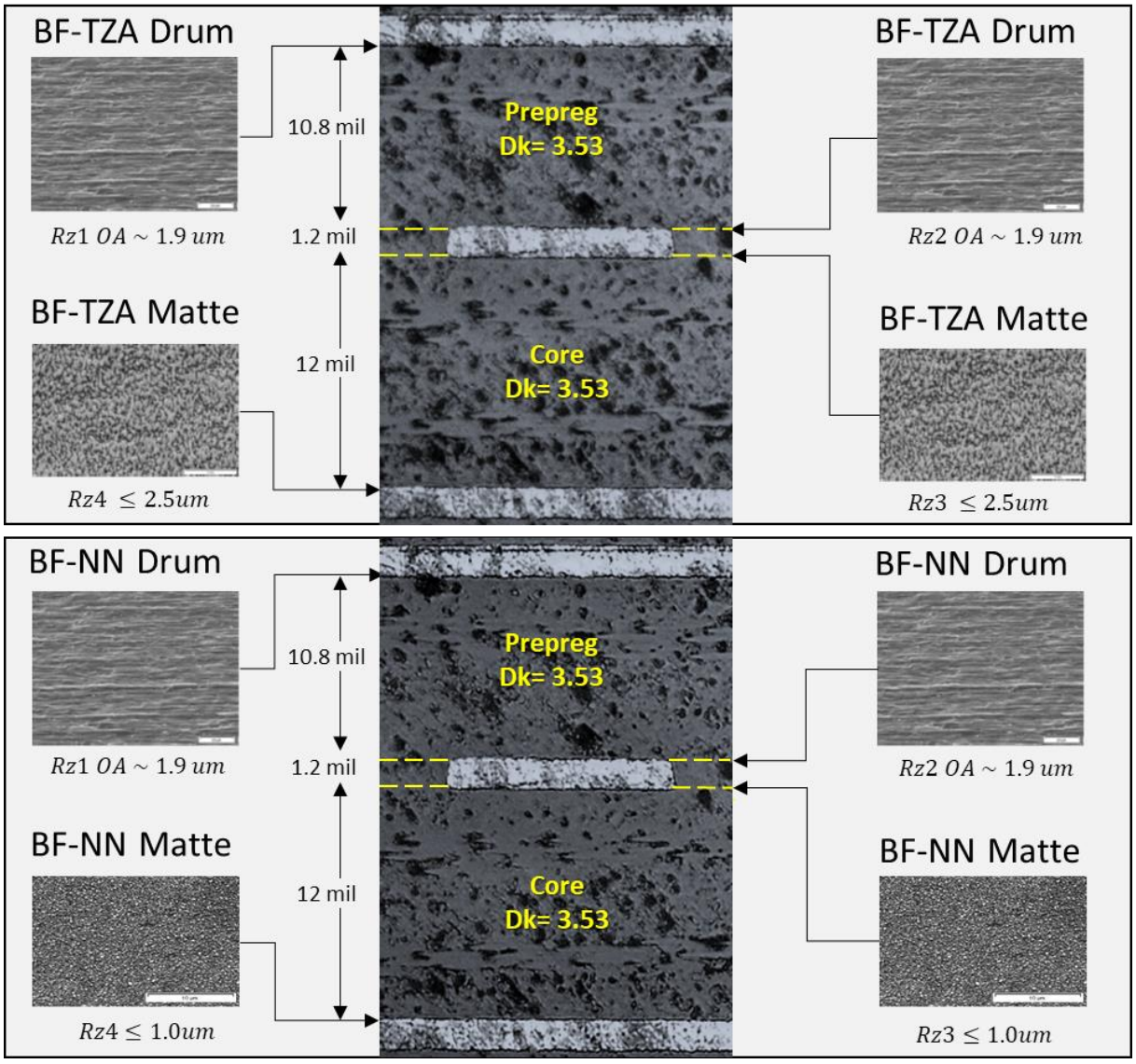


Figure 14 Alternate foil options simulated for what-if loss comparison. Top is VLP2/VLP2 foil parameters for all copper layers and bottom is VLP1/VLP1 foil parameters for all copper layers. Note: Photos are for illustrative purposes only and are not actual cross-section from CMP PCB. Surface roughness pictures source: Circuit Foil [7]

Figure 15 presents the simulation results of all three scenarios. As expected. when the reference plane foil roughness went from RTF/VLP2 to VLP2/VLP2 there was improvement. At 14 GHz it was 0.5 dB and at 28GHz it was 1 dB improvement.

When VLP1/VLP1 foil was used, it was further improved by 0.8 dB and 1.7 dB at 14 GHz and 28 GHz respectively. So if your design is loss sensitive, you might want to consider VLP1 foil option.

When we compare Dkeff plots, we see effective Dk approaches actual Dk/Df data sheet values in the tables when smoother copper is used, as expected [4].

Since Dkeff was derived by phase delay from Equation 8, propagation delay will be affected by rougher copper.

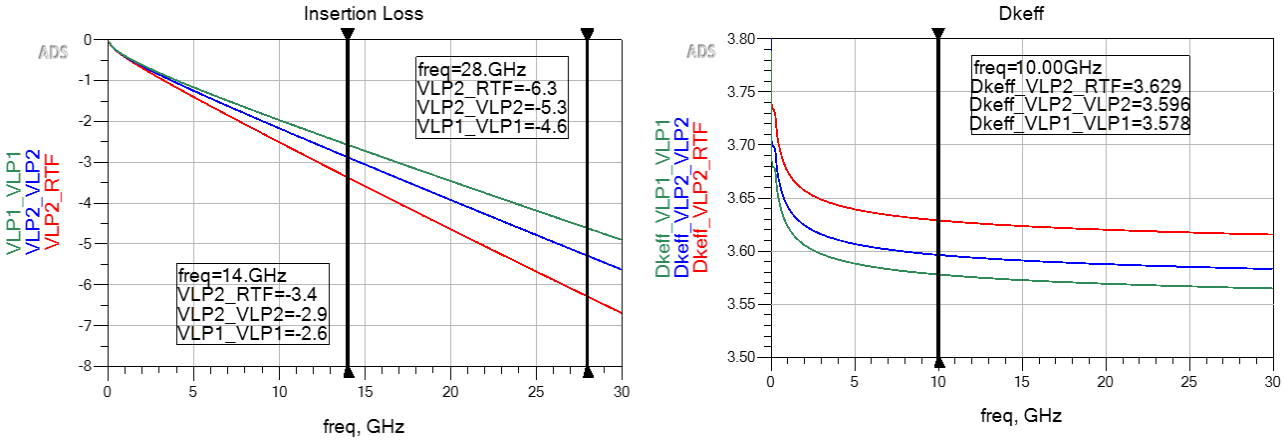


Figure 15 What-if simulation comparison of VLP2/RTF, VLP2/VLP2, VLP1/VLP1 foil options and their effect on insertion loss and Dkeff

Conclusions

1. Heuristic HLD modeling method is a useful and accurate way to determine prefabrication impedance and loss predictions using data sheet parameters.

2. Roughness of reference planes make a significant difference in loss and phase delay, especially if one of the reference planes is RTF. If loss is important then all high-speed reference planes should have the same foil roughness specified.

3. Published Dk from I-Tera® MT40 Dk/Df data sheet tables is not a flat constant over frequency.

4. Confirmed RzJIS is the right parameter to use from Circuit Foil data sheet, instead of RzISO.

Acknowledgements

- Al Neves, CTO Wildriver Technology, for providing the custom modeling platform design details and measured data for the case study.

- Michael Gay, Director Business Development - Strategic Accounts at Isola Group, for providing foil supplier's data sheets used on I-Tera® MT40 laminates.

References

[1] B. Simonovich, "Practical Method for Modeling Conductor Surface Roughness Using The Cannonball Stack Principle", White Paper, Issue 1.0, April 8, 2015

[2] L. Simonovich, "Practical method for modeling conductor roughness using cubic close-packing of equal spheres," 2016 IEEE International Symposium on Electromagnetic Compatibility (EMC), 2016, pp. 917-920, doi: 10.1109/ISEMC.2016.7571773.

[3] L. Simonovich, "PCB Interconnect Modeling Demystified", DesignCon 2019, Proceedings, Santa Clara, CA, 2019

[4] B. Simonovich, "A Practical Method to Model Effective Permittivity and Phase Delay Due to Conductor Surface Roughness". DesignCon 2017, Proceedings, Santa Clara, CA, 2017

[5] Isola Group S.a.r.l., 3100 West Ray Road, Suite 301, Chandler, AZ 85226. URL: http://www.isola-group.com/

[6] Wild River Technology LLC 8311SW Charlotte Drive Beaverton, OR 97007. URL: https://wildrivertech.com/

[7] Circuit Foil, 6 Salzbaach, 9559 Wiltz, Grand Duchy of Luxembourg URL: https://www.circuitfoil.com/

[8] Polar Instruments Si9000e [computer software] Version 2018, URL: https://www.polarinstruments.com/index.html

[9] J.A. Marshall, presented at IPC APEX 2015 titled, "*Measuring Copper Surface Roughness for High Speed Applications*"

[10] High Density Packaging User Group International Inc. URL: http://hdpug.org/smooth-copper-signal-integrity

[11] Keysight Pathwave Advanced Design System (ADS) [computer software], (Version 2021 update2). URL: http://www.keysight.com/en/pc-1297113/advanced-design-system-ads?cc=US&lc=eng.

[12] ANSYS Inc., [computer software], URL: https://www.ansys.com/

[13] Cadence Design Systems Limited, [computer software], URL: https://www.cadence.com/

[14] Mentor Hyperlynx [computer software] URL: https://www.mentor.com/pcb/hyperlynx/

[15] Simberian Inc., 2629 Townsgate Rd., Suite 235, Westlake Village, CA 91361, USA, URL: http://www.simberian.com/

[16] IPC-TM-650 Test Methods Manual 2.2.17A, Surface Roughness and Profile of Metallic Foils (Contacting Stylus Technique), 2/2001 Rev. A

[17] IPC-TM-650, 2.5.5.5, Rev C, Test Methods Manual

[18] Macdermid Enthone, Multibond MP, Inner Layer Oxide Alternative Bonding. URL: https://electronics.macdermidenthone.com/products-and-applications/printed-circuit-board/surface-treatments/innerlayer-bonding

Appendix

isola

I-Tera® MT40

Very Low-Loss Laminate Material

Revision No: G

Dielectric Constant(Dk) / Dissipation factor (Df) Table

Core Data

Construction	Resin Content %	Offering	Thickness (inch)	Thickness (mm)	Dielectric Constant (DK)/ Dissipation Factor (DF)					
					1 GHz	2 GHz	5 GHz	10 Ghz	15 GHz	20 GHz
1x1067	65.5%	Standard	0.0020	0.051	3.26 0.0025	3.26 0.0025	3.26 0.0025	3.26 0.0025	3.26 0.0025	3.26 0.0025
1x1067	71.0%	Standard	0.0025	0.064	3.17 0.0023	3.17 0.0023	3.17 0.0023	3.17 0.0023	3.17 0.0023	3.17 0.0023
1x1078	64.0%	Standard	0.0030	0.076	3.33 0.0027	3.33 0.0027	3.33 0.0027	3.33 0.0027	3.33 0.0027	3.33 0.0027
1x1080	65.0%	Alternate	0.0030	0.076	3.31 0.0026	3.31 0.0026	3.31 0.0026	3.31 0.0026	3.31 0.0026	3.31 0.0026
1x1086	65.0%	Standard	0.0035	0.089	3.29 0.0026	3.29 0.0026	3.29 0.0026	3.29 0.0026	3.29 0.0026	3.29 0.0026
1x3313	55.0%	Standard	0.0040	0.102	3.53 0.0032	3.53 0.0032	3.53 0.0032	3.53 0.0032	3.53 0.0032	3.53 0.0032
2x1035	65.5%	Standard	0.0040	0.102	3.26 0.0025	3.26 0.0025	3.26 0.0025	3.26 0.0025	3.26 0.0025	3.26 0.0025
1x2116	54.5%	Standard	0.0050	0.127	3.56 0.0033	3.56 0.0033	3.56 0.0033	3.56 0.0033	3.56 0.0033	3.56 0.0033
2x1067	70.5%	Standard	0.0050	0.127	3.18 0.0023	3.18 0.0023	3.18 0.0023	3.18 0.0023	3.18 0.0023	3.18 0.0023
2x1078	64.0%	Alternate	0.0060	0.152	3.38 0.0027	3.38 0.0027	3.38 0.0027	3.38 0.0027	3.38 0.0027	3.38 0.0027
2x1080	64.5%	Alternate	0.0060	0.152	3.33 0.0026	3.33 0.0027	3.33 0.0027	3.33 0.0027	3.33 0.0027	3.33 0.0027
2x1086	61.0%	Standard	0.0060	0.152	3.32 0.0028	3.32 0.0028	3.32 0.0028	3.32 0.0028	3.32 0.0028	3.32 0.0028
2x3313	55.0%	Standard	0.0080	0.203	3.53 0.0032	3.53 0.0032	3.53 0.0032	3.53 0.0032	3.53 0.0032	3.53 0.0032
2x3313	59.0%	Alternate	0.0090	0.229	3.43 0.0030	3.43 0.0030	3.43 0.0030	3.43 0.0030	3.43 0.0030	3.43 0.0030
2x3313	63.0%	Alternate	0.0100	0.254	3.36 0.0028	3.36 0.0028	3.36 0.0028	3.36 0.0028	3.36 0.0028	3.36 0.0028
3x3313	55.0%	Alternate	0.0120	0.305	3.53 0.0032	3.53 0.0032	3.53 0.0032	3.53 0.0032	3.53 0.0032	3.53 0.0032
2x2116/1086	55.5%	Alternate	0.0133	0.338	3.51 0.0032	3.51 0.0032	3.51 0.0032	3.51 0.0032	3.51 0.0032	3.51 0.0032

Figure 16 I-Tera® MT40 Dk/Df core data sheet.

Prepreg Dielectric Constant(Dk) / Dissipation factor (Df) Table

Prepreg Data

Glass Style	Resin content %	Standard/ alternate	Thickness (inch)	Thickness (mm)	Dielectric Constant (DK)/ Dissipation Factor (DF)					
					1 GHz	2 GHz	5 GHz	10 GHz	15 GHz	20 GHz
1035	65.5%	Alternate	0.0020	0.051	3.30 0.0028	3.30 0.0028	3.30 0.0028	3.30 0.0028	3.30 0.0028	3.30 0.0028
1035	67.0%	Standard	0.0022	0.056	3.28 0.0026	3.28 0.0026	3.28 0.0026	3.28 0.0026	3.28 0.0026	3.28 0.0026
1067	69.0%	Standard	0.0024	0.061	3.24 0.0024	3.24 0.0024	3.24 0.0024	3.24 0.0024	3.24 0.0024	3.24 0.0024
1067	72.0%	Standard	0.0026	0.066	3.17 0.0022	3.17 0.0022	3.17 0.0022	3.17 0.0022	3.17 0.0022	3.17 0.0022
1035	73.0%	Standard	0.0027	0.069	3.14 0.0022	3.14 0.0022	3.14 0.0022	3.14 0.0022	3.14 0.0022	3.14 0.0022
1067	76.0%	Standard	0.0032	0.081	3.08 0.0020	3.08 0.0020	3.08 0.0020	3.08 0.0020	3.08 0.0020	3.08 0.0020
1086	65.0%	Standard	0.0035	0.089	3.33 0.0027	3.33 0.0027	3.33 0.0027	3.33 0.0027	3.33 0.0027	3.33 0.0027
1080	70.0%	Standard	0.0037	0.094	3.21 0.0024	3.21 0.0024	3.21 0.0024	3.21 0.0024	3.21 0.0024	3.21 0.0024
1078	69.0%	Standard	0.0037	0.094	3.24 0.0024	3.24 0.0024	3.24 0.0024	3.24 0.0024	3.24 0.0024	3.24 0.0024
1086	68.0%	Standard	0.0039	0.099	3.26 0.0025	3.26 0.0025	3.26 0.0025	3.26 0.0025	3.26 0.0025	3.26 0.0025
3313	57.0%	Alternate	0.0043	0.109	3.53 0.0033	3.53 0.0033	3.53 0.0033	3.53 0.0033	3.53 0.0033	3.53 0.0033
1080	73.0%	Standard	0.0042	0.107	3.14 0.0022	3.14 0.0022	3.14 0.0022	3.14 0.0022	3.14 0.0022	3.14 0.0022
1078	73.0%	Alternate	0.0043	0.109	3.14 0.0022	3.14 0.0022	3.14 0.0022	3.14 0.0022	3.14 0.0022	3.14 0.0022
1086	71.0%	Alternate	0.0044	0.112	3.19 0.0023	3.19 0.0023	3.19 0.0023	3.19 0.0023	3.19 0.0023	3.19 0.0023
1078	75.0%	Standard	0.0047	0.119	3.10 0.0020	3.10 0.0020	3.10 0.0020	3.10 0.0020	3.10 0.0020	3.10 0.0020
1080	75.0%	Alternate	0.0046	0.117	3.10 0.0020	3.10 0.0020	3.10 0.0020	3.10 0.0020	3.10 0.0020	3.10 0.0020
3313	61.0%	Standard	0.0048	0.122	3.43 0.0030	3.43 0.0030	3.43 0.0030	3.43 0.0030	3.43 0.0030	3.43 0.0030
3313	63.0%	Alternate	0.0050	0.127	3.36 0.0028	3.36 0.0028	3.36 0.0028	3.36 0.0028	3.36 0.0028	3.36 0.0028
3313	64.0%	Standard	0.0053	0.135	3.36 0.0028	3.36 0.0028	3.36 0.0028	3.36 0.0028	3.36 0.0028	3.36 0.0028
2116	59.0%	Standard	0.0057	0.145	3.48 0.0031	3.48 0.0031	3.48 0.0031	3.48 0.0031	3.48 0.0031	3.48 0.0031

Figure 17 I-Tera® MT40 Dk/Df prepreg data sheet

HIGH FREQUENCY

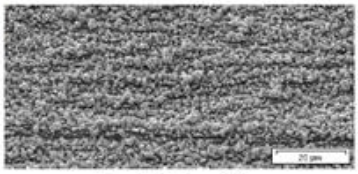
TWLS-B

HIGH BOND REVERSE TREATED COPPER FOIL ON HYDROCARBON SUBSTRATES.

IPC Grade 3 | 33 As Arsenic | REVERSE TREATED RTF

TYPICAL SUBSTRATES

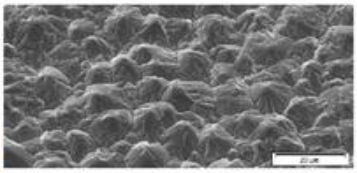
Hydrocarbon, Polyphenylene Ether/Oxide (PPE / PPO) based, high Tg and highly filled resin systems.



Treated Drum Side

TYPICAL PROCESSES

Radio frequency, microwave and high speed digital multilayer Printed Circuit Boards.



Untreated Electrolyte Side

TYPICAL APPLICATIONS

Base stations infrastructures, automotive radars and digital applications.

*TYPICAL AVERAGE PROPERTIES**

TWLS-B

MEASURED PARAMETERS		UNITS	PRODUCT GAUGE			IPC	
Nominal Thickness		µm oz.	18 1/2	35 1	70 2	Specification IPC-4562A	Test Method IPC-TM-650
Area weight		g/m²	157	287	577	3.4.4	2.2.12
Untreated Matte Side Roughness (Rz)	JIS	µm	≤ 5.0	≤ 7.5	≤ 9.2	-	2.2.17
	ISO		≤ 6.0	≤ 9.0	≤ 11.0	3.4.5	
Treated Shiny Side Roughness (Rz)	JIS		≤ 4.2			-	
	ISO		≤ 5.1			3.4.5	
Tensile Strength Transverse (RT)		MPa (k.Lb/in²)	≥ 276 (≥ 40)			3.5.1	2.4.18
Tensile Strength Transverse (180 °C)			≥ 138 (≥ 20)				
Elongation Transverse (RT)		%	≥ 6	≥ 9	≥ 12	3.5.3	
Elongation Transverse (180 °C)			≥ 3				
Peel Strength Filled Hydrocarbon Resin[1] (RT)		N/mm (Lb/in)	≥ 0.5 (≥ 2.9)	≥ 0.6 (≥ 3.4)		3.5.4	2.4.8

[1] Laminate construction with thickness ≥ 0.5 mm

ALTERNATIVE For matte-side treated type please consult TWLS datasheet.
For fluoropolymer resin system please consult HFA-B datasheet.

* ALL OF THIS TECHNICAL INFORMATION HAS BEEN DETERMINED WITH DUE CARE AND THOROUGHNESS. HOWEVER, BECAUSE THE CONDITIONS OF USE AND PROCESS AND APPLICATION TECHNOLOGIES EMPLOYED CAN SUBSTANTIALLY VARY, THE PROVIDED DATA AND FIGURES CAN ONLY SERVE AS NON-BINDING GUIDELINES. THEY DO NOT CONSTITUTE A GUARANTEE THAT THE PURCHASED ITEM WILL POSSESS CERTAIN ATTRIBUTES. FOR THIS REASON, NO LIABILITY WHATSOEVER CAN BE ASSUMED FOR THEM. THE BUYER IS OBLIGED TO CHECK THE SUITABILITY OF ALL SUPPLIED PRODUCTS.

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CIRCUIT FOIL

Figure 18 Circuit Foil TWLS-B (Isola's RTF) data sheet

HIGH SPEED DIGITAL & HDI

BF-TZA

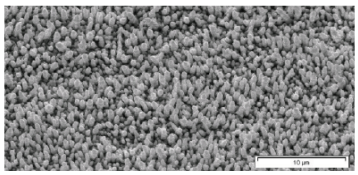
ULTRA FLAT COPPER FOIL FOR REDUCED SIGNAL LOSSES.

IPC Grade 10 & 3

33 As Arsenic 74.92

TYPICAL SUBSTRATES

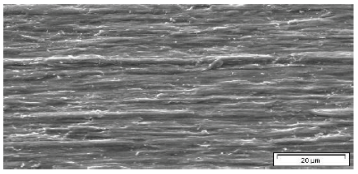
Very low loss substrates including Polyphenylene Ether/Oxide (PPE / PPO) based resin systems.



Treated Electrolyte Side

TYPICAL PROCESSES

High speed digital Printed Circuit Board.
The ultra flat profile surface structure helps mitigating the impact of the skin effect.



Untreated Drum Side

TYPICAL APPLICATIONS

Networking and communication infrastructures including routers, switches and servers.

*TYPICAL AVERAGE PROPERTIES**

BF-TZA										
MEASURED PARAMETERS			**UNITS**	**PRODUCT GAUGE**					**IPC**	
Nominal Thickness			**µm oz.**	**9 1/4**	**12 3/8**	**18 1/2**	**35 1**	**70 2**	**Specification IPC-4562A**	**Test Method IPC-TM-650**
Area Weight			g/m²	79	112	152	285	574	3.4.4	2.2.12
Untreated Side Contact Roughness	Ra	ISO 4287	µm	≤ 0.35					3.5.6	2.2.17
Untreated Side Contactless Roughness	Sa	ISO 25178	µm	~ 0.22					-	2.2.22 Draft[2]
Treated Side Contact Roughness	Rz	JIS B 601	µm	≤ 2.5				≤ 2.0	-	2.2.17
	Rz	ISO 4287	µm	≤ 3.1				≤ 2.5	3.4.5	
Treated Side Contactless Roughness	Sa	ISO 25178	µm	~ 0.42	~ 0.38	~ 0.35	~ 0.31	~ 0.26	-	2.2.22 Draft[2]
	Sz		µm	~ 4.7	~ 4.4	~ 4.1	~ 3.7	~ 3.3		
	Sdr		%	~ 12	~ 11.5	~ 11	~ 10.5	~ 10		
Tensile Strength Transverse (RT)			MPa (k.Lb/in²)	≥ 276 (≥ 40)					3.5.1	2.4.18
Elongation Transverse (RT)			%	4 - 14	5 - 15	7 - 25	10 - 35	15 - 40	3.5.3	
Peel Strength Very Low Loss (PPE Based Resin)[1] (RT)			N/mm (Lb/in)	≥ 0.6[3] (≥ 3.4)	≥ 0.45 (≥ 2.6)	≥ 0.5 (≥ 2.9)	≥ 0.6 (≥ 3.4)	≥ 0.7 (≥ 4.0)	3.5.4	2.4.8

[1] Laminate construction with thickness ≥ 0.5 mm
[2] Final draft of TM 2.2.22 as of Sept. 29th, 2015
[3] After build-up to 35 µm

ALTERNATIVE For reduced conductor losses consult BF-ANP and BF-NN datasheets.

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CIRCUIT FOIL

Figure 19 Circuit Foil BF-TZA (Isola's VLP2) standard foil data sheet for I-Tera® MT40

HIGH SPEED DIGITAL & HIGH FREQUENCY

BF-NN / BF-NN-HT

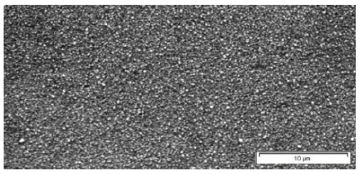
SUPER FLAT PROFILE COPPER FOIL FOR REDUCED SIGNAL LOSSES. BF-NN-HT VERSION WITH HIGHER THERMAL RELIABILITY IS ALSO AVAILABLE.

IPC Grade 10 & 3

33 As Arsenic 74.92

TYPICAL SUBSTRATES

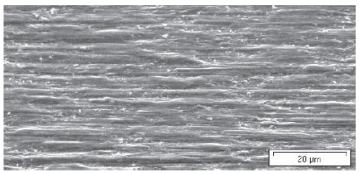
Ultra low loss substrates including Polyphenylene Ether/Oxide (PPE / PPO) based resin systems.
Also convenient for pure or modified fluoropolymer (PTFE) resin systems.



Treated Electrolyte Side

TYPICAL PROCESSES

Radio frequency, microwave and high speed digital Printed Circuit Boards.
The super flat profile surface structure helps mitigating the impact of the skin effect.
The pure copper treatment supports reducing the passive intermodulation (PIM).



Untreated Drum Side

TYPICAL APPLICATIONS

Networking and communication infrastructures including routers, switches and servers especially for 5G.
Also used for base stations infrastructures and 77 GHz automotive radars.

*TYPICAL AVERAGE PROPERTIES**

BF-NN / BF-NN-HT

MEASURED PARAMETERS			UNITS	PRODUCT GAUGE				IPC	
Nominal Thickness			µm oz.	9 1/4	12 3/8	18 1/2	35 1	Specification IPC-4562A	Test Method IPC-TM-650
Area Weight			g/m²	71	100	143	277	3.4.4	2.2.12
Untreated Side Contact Roughness	Ra	ISO 4287	µm	≤ 0.3				3.5.6	2.2.17
Untreated Side Contactless Roughness	Sa	ISO 25178	µm	~ 0.20				-	2.2.22 Draft[2]
Treated Side Contact Roughness	Rz	JIS B 601	µm	≤ 1.4	≤ 1.2	≤ 1.1	≤ 1.0	-	2.2.17
	Rz	ISO 4287	µm	≤ 1.8	≤ 1.6	≤ 1.4	≤ 1.3	3.4.5	
Treated Side Contactless Roughness	Sa	ISO 25178	µm	-	~ 0.18	~ 0.16	~ 0.14	-	2.2.22 Draft[2]
	Sz		µm	-	~ 2.3	~ 1.7	~ 1.5		
	Sdr		%	-	~1.4	~ 1.1	~ 0.8		
Tensile Strength Transverse (RT)			MPa (k.Lb/in²)	≥ 276 (≥ 40)				3.5.1	2.4.18
Elongation Transverse (RT)			%	4 - 14	5 - 15	7 - 25	10 - 35	3.5.3	
Peel Strength Very Low Loss (PPE Based Resin)[1] (RT)			N/mm (Lb/in)	≥ 0.6[3] (≥ 3.4)	≥ 0.35 (≥ 2.0)	≥ 0.4 (≥ 2.3)	≥ 0.5 (≥ 2.9)	3.5.4	2.4.8

[1] Laminate construction with thickness ≥ 0.5 mm

[2] Final draft of TM 2.2.22 as of Sept. 29th, 2015

[3] After build-up to 35 µm

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CIRCUIT FOIL

Figure 20 Circuit Foil BF-NN (Isola's optional VLP1) smoother foil data sheet for I-Tera® MT40